IN THE CLAIMS:

1. (currently amended) An integrated circuit including a multi-layered barrier metal thin film structure, comprising:

a substrate;

a first barrier ~~metal~~ thin film deposited on said substrate by the process of atomic layer chemical vapor deposition (ALCVD);

a second barrier ~~metal~~ thin film deposited by ALCVD;

a thin copper film deposited on said second barrier ~~metal~~ thin film; and,

wherein said first barrier ~~metal~~ thin film and said second barrier ~~metal~~ thin film are each chosen from the group consisting of TiN, TaN, W, WN, and Si_3N_4.

2. (currently amended) The integrated circuit of claim 1 wherein said first and second barrier ~~metal~~ thin films define[[s]] a thickness in a range of 50 to 100 Angstroms.

3. (currently amended) The integrated circuit of claim 1 wherein said first barrier ~~metal~~ thin film defines a thickness equal to an atomic thickness of said first barrier ~~metal~~ thin film.

4-6. canceled

7. (currently amended) The integrated circuit of claim 1 wherein said substrate comprises a trench having a bottom surface and a side wall, and wherein said first barrier ~~metal~~ thin film is deposited on said bottom surface and said side wall by atomic layer

chemical vapor deposition such that said first barrier ~~metal~~ thin film defines a blocking diffusion characteristic which is the same on said side wall and said bottom surface.

8-20. canceled

21. (new) The integrated circuit of claim 1 wherein said second barrier thin film defines a thickness equal to an atomic thickness of said second barrier thin film.